Sabeeka Fatima

Islamabad, Islamabad Capital Territory, Pakistan | sabeekafatima84@gmail.com | 03193457488 | LinkedIn

Professional Summary

- As a graduate researcher in Computer Engineering, my MS research focuses on AI-driven signal detection for MIMO systems in next-generation 6G wireless networks, with an emphasis on deep learning-based detection under realistic propagation conditions.
- Complementing my research, I have hands-on training in digital design verification, RTL development, and ASIC design flows, with experience in SystemVerilog, UVM, and Cadence tools for functional verification, synthesis, physical design, timing analysis, and hardware optimization.
- My research interests lie at the intersection of artificial intelligence, next-generation wireless communications, and chip design, particularly in hardware-aware AI, efficient AI accelerators, edge AI, intelligent signal-processing architectures, and algorithm–hardware co-design for scalable, energy-efficient, and reliable 6G systems.

Education

MS Computer Engineering | National University of Science and Technology, Islamabad [2024- 2026]
Dissertation Title: AI-Driven Signal Detection for MIMO Systems in 6G Networks
Advisors: Dr. Kiran Khurshid [LINK] & Dr. Muhammad Usman Akram [LINK] & Dr. Farhan Hussain [LINK]

BS Computer Engineering | Comsats University Islamabad, Islamabad [2024]
Project Title: Human Facial Expression Recognition Using Neural Networks
Advisor: Dr. Atif Shakeel [LINK]

Research Experience

Digital Design & Verification Trainee | NUST Chip Design Centre (NCDC), Islamabad [2025]

- Designed and verified digital systems and IP blocks, including RISC-V processors, UART, FIFO, and SPI interfaces, using SystemVerilog and UVM.
- Developed constrained-random UVM verification environments incorporating functional coverage and SystemVerilog Assertions for comprehensive functional and protocol verification.
- Performed RTL synthesis, static timing analysis, timing optimization, and timing closure for single- and multi-clock digital designs using Cadence Genus.
- Executed the RTL-to-GDSII physical design flow, including floorplanning, placement, clock tree synthesis, routing, and power, performance, and area optimization using Cadence Innovus.
- Performed Design-for-Test and scan-chain insertion and validation, supporting testability and structural verification of processor-based designs.
- Conducted RTL and gate-level simulation, waveform analysis, and systematic debugging of functional and timing issues using Cadence Xcelium.

Professional Experience

Student Intern | Press Network of Pakistan (PNP), Islamabad **Mar 2024 — May 2024**

- Supported editorial and administrative operations including scheduling, coordination, and documentation
- Assisted in organizing reports, conducting fact-checking, and managing information flow
- Coordinated with team members to meet deadlines in a fast-paced environment
- Maintained organized records and ensured timely communication across teams

Interviewer Officer | Times Consultant (Pvt.) Ltd., Islamabad **Jun 2024 — Aug 2024**

- Conducted structured interviews and managed candidate documentation for international applications
- Maintained and updated CRM systems, ensuring accurate and organized records
- Coordinated with internal teams to streamline application workflows and improve efficiency
- Handled sensitive applicant information with confidentiality and professionalism

Leadership Experience

Sustainable Tourism Ambassador | Young Leaders Convention, Turkey **August - 2023**

- Represented Pakistan at an international youth leadership convention
- Contributed to discussions on sustainable tourism and responsible development
- Collaborated with diverse global participants to promote eco-friendly travel practices and cross-cultural cooperation
- Participated in structured sessions, group initiatives, and leadership forums

Event Manager | COMSATS University Islamabad **January - 2024**

- Managed end-to-end coordination of a two-day international academic conference
- Handled scheduling, logistics, and communication with speakers and participants
- Served as the primary liaison between stakeholders, ensuring smooth event execution
- Resolved issues in real-time to maintain workflow efficiency

Treasurer CUI Tech Summit | COMSATS University Islamabad **March - 2024**

- Managed budgeting, expense tracking, and financial documentation for a large-scale event
- Coordinated with vendors, sponsors, and internal teams for timely payments
- Maintained accurate financial records and ensured transparency

Technical Skills

HARDWARE	**Digital Design & Verification**	RISC-V, UART, FIFO, SPI, ASIC Design Flow
	Hardware Languages	SystemVerilog, Verilog
	Verification	UVM, SVA, Constrained-Random Verification, Functional Coverage
	Synthesis & Timing	Static Timing Analysis (STA), Timing Closure
	Physical Design	Floorplanning, Placement, Clock Tree Synthesis, Routing
SOFTWARE	**EDA Tools**	Cadence Xcelium, Genus, Innovus
	Simulation & Development	ModelSim (basic), MATLAB (basic)
COMPUTER	**Programming Languages**	Python, C, C++
	Scripting Languages	Bash, Makefiles
PLATFORMS		Linux (Red Hat), Windows
MISC		PyTorch (Deep Learning), Git, LaTeX, MS Office

Projects

Title	Software	Hardware	Programming Language
Design and Verification of RISC-V Single-Cycle Processor	Cadence Xcelium, Genus, Innovus	ASIC	SystemVerilog
HEVC CABAC Encoder Verification using UVM	Cadence Xcelium, Python	ASIC	SystemVerilog, Python
ASIC Design Flow of RISC-V Processor (Front-end & Back-end)	Cadence Genus, Innovus	ASIC	SystemVerilog
UART Controller Design and Timing Closure	Cadence Xcelium, Genus	ASIC	SystemVerilog
Verification of FIFO and SPI Interfaces using UVM	Cadence Xcelium	ASIC	SystemVerilog
Cache Simulator and Architecture Exploration (Direct-Mapped & Set-Associative)	C Compiler (GCC)	-	C

Title	Software	Hardware	Programming Language
FPGA-Based 7-Segment Display and Barrel Shifter Design	Xilinx ISE / Vivado	FPGA (Nexys A7)	SystemVerilog

Certificates

Certificate of Participation | ROBOCI (Sumo Robot Competition)
Collaborated in a team to design and program a Sumo Robot, achieving reliable performance through optimized control and sensing mechanisms

Certificate of Merit | BS Computer Engineering
Awarded for securing 3rd position in class after completion of 2nd semester

Research Interests

- AI hardware accelerators and energy-efficient architectures for intelligent computing and signal processing
- Machine learning-enabled hardware and hardware-aware AI for next-generation communication systems
- AI-driven signal detection for MIMO, mm-Wave, and next-generation wireless communication systems
- RF/mm-Wave communication systems and intelligent signal processing
- Algorithm–hardware co-design for scalable and energy-efficient AI and communication systems
- Digital IC design, RTL design and verification, and ASIC system design
- Emerging computing and communication architectures for AI-enabled wireless systems

References

Dr. Kiran Khurshid (MS Supervisor)
Assistant Professor, Department of Computer & Software Engineering, CEME, NUST, Islamabad, Pakistan
Email: kiran.khurshid@ceme.nust.edu.pk **Google Scholar:** Kiran Khurshid

Dr. Muhammad Usman Akram
Head, Department of Computer & Software Engineering, CEME, NUST, Islamabad, Pakistan
Email: usman.akram@ceme.nust.edu.pk **Google Scholar:** Muhammad Usman Akram